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2004.7.26

Via Federal Express
Noboru Otsuka
Hitachi, Ltd.
IP Development & Management Division
Patent Dept. 4
292, Yoshida-cho, Totsuka, Yokohama-shi

Kanagawa, Japan 244-0817

RE: PATENTABILITY SEARCH FOR STORAGE DEVICE CONTROLLING DEVICE AND CONTROL METHOD FOR STORAGE DEVICE CONTROLLING DEVICE
Your File: 340300908US01
Our Docket: PSP-1041617

Dear Mr. Otsuka:

In accordance with your request, we have conducted a patentability search on the above-identified subject matter.

Enclosed with this report are copies of the search results and your disclosure materials. If after reviewing the results, you feel that the search feature (or specific search elements), the field of search, or results are not commensurate with your original request, or you would like to extend the search into additional areas, please contact us.

Sincerely,

R W Lacasse

Randy W. Lacasse

Enclosures
RWL:NC:pd
s04/psp1041617

CONFIDENTIAL
(Patentability Search)

I. SEARCH FEATURE

A storage device controlling device comprising:

a channel controller for receiving a data input/output request based on file-name indication from an information processing device through a network and transmitting/receiving data to/from the information processing device;

a disk controller for carrying out input/output control of data stored in a storage volume for storing the data; and

a first memory for storing the data delivered between the channel controller and the disk controller, wherein the channel controller is equipped with a first processor for outputting a block-basis I/O request corresponding to the data input/output request and controlling the first memory, a file access processor which has a second processor and a second memory controlled by the second processor and serves to control the transmission/reception of the data input/output request and the data which is carried out with the information processing device, a data transfer device for controlling data transfer between the first memory and the second memory, and a third memory controlled by the first processor, which are formed on a circuit, and wherein the second processor transmits information indicating the storage position of the data in the second memory to the first processor, the first processor writes into the third memory data transfer information containing information indicating the storage position of the data in the first memory and information indicating the storage position of the data in the second memory, and the data transfer device reads out the data transfer between the first memory and the second memory on the basis of the data transfer information thus read out.

II. FIELD OF SEARCH

The search of the above features was conducted in the following areas:

A. Classification search

Class	Subclasses	Description
710/		**ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT**
	8	. Peripheral configuration
711/		**ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY**

100	STORAGE ACCESSING AND CONTROL
112	... Direct access storage device (DASD)
117	. Hierarchical memories
118	.. Caching
147	. Shared memory area

The above subclasses represent areas deemed to contain subject matter of interest to one or more of the search features. Please note that relevant references may be classified outside of these areas. The integrity of the search is based on the records as presented to us by the United States Patent and Trademark Office (USPTO). No further integrity studies were performed. Also a key word search was performed on the USPTO full-text database including published U.S. patent applications.

III. RESULTS OF SEARCH

A. References developed as a result of search (related art is in boldface):

U.S. Patent No.	Inventor
6,516,390 B1	**Chilton et al.**
6,646,947 B2	**Fukui et al.**

U.S. Patent Application Publication No.	Inventor
2003/0023784 A1	**Matsunami et al.**
2004/0128456 A1	**Kobayashi et al.**
2004/0139168 A1	**Tanaka et al.**

Foreign Patent No.	Inventor
JP2003345515	**Fujimoto et al.**

B. Discussion of related references in numerical order:

The patent to Chilton et al. (6,516,390 B1), assigned to EMC Corporation provides for *Methods and Apparatus for Accessing Data within a Data Storage System*. The storage system includes a buffer circuit interconnected between a front-end circuit and a back-end circuit residing on a circuit board. The buffer circuit includes a multi-port memory and cache interface logic. The buffer circuit provides a direct path between the front-end and back-end circuits (see column 5, lines 14-20; column 7, lines 6-8, 18-21, and 28-31; and column 9, lines 59-66).

The patent to Fukui et al. (6,646,947 B2), assigned to Sharp Kabushiki Kaisha provides for a *Data Transfer Control Device Semiconductor Memory Device and Electronic Information Apparatus*. Discussed is a method of controlling data transfer between first and second memory arrays based on an input control command and data transfer start addresses stored in first and second memories and data transfer completion address output from the first address output section stored in the third memory section (see column 4, lines 25-49).

The patent application publication to Matsunami et al. (2003/0023784 A1), assigned to Hitachi, Ltd. provides for a *Storage System Having a Plurality of Controllers*. This application generally describes a storage system comprised of a plurality of disk array controllers and file servers.

The patent application publication to Kobayashi et al. (2004/0128456 A1), assigned to Hitachi, Ltd. provides for a *Storage System and Data Backup Method for the same*. The storage system comprises a network adapter including a first processor that receives a file access request and a third processor that receives an access to data stored in the storage device, a channel adapter including a second processor for sending data stored in the storage device and a disk adapter for accessing data stored in the storage device (see paragraphs 31, 33, 53, and 54).

The patent application publication to Tanaka et al. (2004/0139168 A1), assigned to Hitachi, Ltd. provides for a *SAN/NAS Integrated Storage System*. The storage system includes controllers with a block and file interfaces to communicate with the host computer. The channel adapter unit and file server unit are disposed on the same circuit board (see paragraphs 41, 43, and 45).

The patent to Fujimoto et al. (JP 2003345515), assigned to Hitachi, Ltd. provides for a *Disk Controller, Storage System, and Method for Controlling the same*. A method of controlling transfer of data between a host and a cache memory, disk device and cache memory and a data transfer adapter means. The data transfer adapter reads the parameter stored in the memory and executes the transfer of data based on the read parameter.

Nidhi Chotani